AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Original) A verification test bench system used in testing in a core which is used in a design which comprises:

a. a bus functional model which comprises a mirror interface to the core and memory;

b. a bi-directional general purpose I/O device; and

c. a control mechanism which comprises:

1) a standardized handshake protocol between the design and the mirror interface; and

2) control code loaded into the bus functional model that controls data flow, transfer direction, and data checking when a test case is running in the design.

2. (Previously presented) The verification test bench system of claim 1, wherein said core has an external interface external to said design, said mirror interface is coupled to said external interface, and said test case issues directives in said handshake protocol to initiate and control an exchange of data between said mirror interface and external interface.

3. (Original) The verification test bench system of claim 2, wherein said bi-directional general purpose I/O device is coupled between said design and said bus functional model, and transfers said directives between said design and said bus functional model.

4. (Original) The verification test bench system of claim 2, wherein said control code responds to said directives by configuring said mirror interface for said exchange of data.

5. (Original) The verification test bench system of claim 4, wherein said control code verifies results of said exchange of data.

6. (Previously presented) A verification system comprising:

a core in a system-on-chip (SOC) design, said core having an external interface external to said SOC;

a copy of said core comprising a mirror interface, said mirror interface coupled to said external interface of said core;

a control mechanism for controlling said mirror interface; and

a test case executing in said SOC which applies verification stimuli to said external interface using said control mechanism.

7. (Original) The verification system of claim 6, said control mechanism comprising:

a standardized handshake protocol for communicating with said SOC; and

control code for configuring said mirror interface and transferring data to said external interface via said mirror interface.

8. (Original) The verification system of claim 7, further comprising communication means coupled between said SOC and said control mechanism for transferring control directives in said handshake protocol from said test case to said control mechanism.

9. (Original) The verification system of claim 8, wherein said test case issues directives for initiating a data transfer between said mirror interface and said external interface.

10. (Original) The verification system of claim 9, wherein said control mechanism configures said mirror interface in response to said directives.

11. (Original) A verification method comprising:

attaching a mirror interface to an external interface of a core in an SOC; and

executing a test case in said SOC which applies test stimuli to said external interface using said mirror interface.

12. (Original) The method of claim 11, further comprising providing a control mechanism for enabling said test case to configure and control said mirror interface.

13. (Original) The method of claim 12, wherein said control mechanism comprises:

a standardized handshake protocol for communicating with said SOC; and

control code for configuring said mirror interface and transferring data to said external interface via said mirror interface.

14. (Original) The method of claim 13, further comprising issuing directives in said handshake protocol to said control code, to configure said mirror interface and initiate data transfer between said mirror interface and said external interface.

15. (Original) The method of claim 11, further comprising connecting a bus functional model to said mirror interface, to provide processor bus cycles for driving said mirror interface.

16. (Original) The method of claim 12, further comprising connecting bi-directional communication means between said SOC and said control mechanism, to enable said test case to communicate with said control mechanism.

17. (Original) A program product tangibly embodied on a computer-usable medium, said program product comprising computer-executable instructions which when executed implement a process comprising the steps of:

connecting an external interface of a core on an SOC to a mirror interface of said external interface; and

executing a test case in said SOC to apply test stimuli for verification of said external interface via said mirror interface.

18. (Original) The program product of claim 17, said process further comprising executing a control mechanism for enabling said test case to control said mirror interface.

19. (Original) The program product of claim 18, said step of executing a control mechanism comprising:

receiving directives issued by said test case in a handshake protocol; and

configuring said mirror interface for an exchange of data with said external interface in response to said directives.

20. (Original) The program product of claim 17, said process further comprising implementing communication means for enabling said test case to communicate with said mirror interface.

21. (New) A system for verifying an external interface of a core of a system on a chip (SOC) comprising:

a mirror interface having the identical input and output connections of said external interface;

a bus functional interface connected to said mirror interface for modeling an internal bus, said bus functional interface having a processor model for emitting CPU cycles which emulate a processor, a control mechanism which controls the flow of data through the external interface and to apply test stimuli from the mirror interface to the external interface, and a memory to receive any data transferred from the external interface; and

an external bi-directional general purpose I/O connected to said SOC to transfer control directives to configure the mirror interface through the bus functional interface for a given test case being executed in said SOC, and to exchange data between the external interface and mirror interface during the given test case.